

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**

BEST AVAILABLE COPY

**Remarks**

Claims 1-7, 10-12, 14-15, and 24-28 are pending in this application. By the foregoing amendment, Applicant seeks to amend claims 1, 10, and 14. These changes are believed to be fully supported by the specification and are not believed to introduce new matter. Thus, it is respectfully requested that the amendments and additions be entered by the Examiner. Based on the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding rejections, and that they be withdrawn.

**Telephone Interview**

Applicant's Representative wishes to thank the Examiner for the telephone interview accorded him on October 25, 2002.

Regarding the Interview Summary, Applicant's representative did not agree during the Interview that claim 14 was shown by U.S. Patent No. 5,852,866 (hereinafter "Kuettner"). Claim 14 includes a pattern of via holes sufficient to couple a varying voltage present along *the length* of the first track on to the second track. As discussed during the Interview (but not agreed to), the feature of coupling a varying voltage present along *the length* of the first track on to the second track, is not shown by Kuettner. Accordingly, Applicant requests that the Interview Summary be corrected to show that no agreement was reached regarding claim 14 at the time of the interview.

It is noted that claim 14 is further amended herein to further define the invention, and to advance prosecution of this application.

**Rejections under 35 U.S.C. § 112**

At paragraphs 1-2, claims 10-12 were rejected under 35 U.S.C. § 112, ¶ 2 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Based on the following remarks and amendments discussed below, the Applicant respectfully traverses this rejection.

Claim 10 has been amended to recite that the  $n^+$  diffusion layer *has a fingered pattern shape with  $n^+$  fingers electrically isolated by regions of polysilicon*. FIG. 28F clearly illustrates one embodiment of claim 10, where  $n^+$  fingers 2866 are separated by polysilicon regions 2868. FIG. 28F is further defined in the specification on page 76, lines 20-35. Accordingly, Applicant asserts that claim 10 is sufficiently definite to meet the requirements of 35 U.S.C. § 112, ¶ 2.

Based on the discussion above, Applicant asserts that claims 10-12 meet the requirements of 35 U.S.C. § 112, ¶ 2, and therefore requests that these rejections be withdrawn.

### ***Rejections under 35 U.S.C. § 103***

At paragraphs 1-6, claims 1-3, 5-7, 10-12, 14, and 24-28 were rejected under 35 U.S.C. § 103 as allegedly being obvious over U.S. Patent No. 5,852,866 to Kuettner *et. al.* (hereinafter "Kuettner"), in view of U.S. Patent No. 5,852,866 to Nasserbakht (hereinafter "Nasserbakht"), and further in view of U.S. Patent No. 5,966,063 to Sato *et. al.* (hereinafter "Sato"). Applicant respectfully traverses this rejection based on the arguments below.

Claim 1 has been amended so that the  $n^+$  diffusion layer is disposed in the substrate *directly underneath* the spiral inductor metalization pattern. As agreed during the Interview, the  $N^+$  diffusion region 42 in FIG. 3 of Nasserbakht is not directly underneath the spiral 32. Furthermore, neither Kuettner or Sato cure this defect. Accordingly, Applicant requests that 35 U.S.C. § 103 rejection be removed, and that claim 1 and the respective dependant claims 2-7 and 10-12 be passed to allowance.

Furthermore, dependent claim 10 is additionally allowable because the cited art does not teach a  $n^+$  diffusion layer that has a fingered pattern shape with  $n^+$  fingers electrically isolated by regions of polysilicon.

As discussed in the Interview, the features of claim 24 are not taught or suggested by Kuettner. For instance, the contacts 24 (FIG. 4 of Kuettner) on one layer are not connected to the contacts 23 on another layer, as is recited in claim 24. Furthermore, Kuettner cannot be modified to connect the contacts 23 and 24 together, because to do so

would short the input directly to the output, which would short-out the coil inductance and defeat the purpose of Kuettner. Accordingly, Applicant requests that 35 U.S.C. § 103 rejection be removed, and that claim 24 and the dependant claims 24-28 be passed to allowance.

Claim 14 has been amended to recite features similar to claim 24. Namely, that the first spiral track on the first layer has *a first input and a first output*, and the second track on the second layer has *a first input and a first output*. The first and second inputs are connected together by a first via hole of the pattern of via holes, and the first and second outputs are connected together by a second via hole of the pattern of via holes.

As discussed in the Interview, FIG. 4 of Kuettner teaches inputs 24 on one layer and outputs 23 on another layer, but not an input and an output on each layer as recited in claim 24. Furthermore, the inputs 24 of Kuettner cannot be connected to the outputs 23, because this would short-out the intended inductor. Accordingly, Applicant requests that 35 U.S.C. § 103 rejection be removed, and that claim 14 be pass to allowance. Claim 15 is allowable for at least the same reasons as discussed herein for claims 14 and 24.

For at least the reasons discussed above, Applicant asserts that independent claims 1, 14, 15, and 24, and their respective dependant claims are allowable over the cited references. Accordingly, Applicant requests that these claims be passed to allowance.

*Conclusion*

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Jeffrey Helvey  
Attorney for Applicants  
Registration No. 44,757

Date: 10/31/02

1100 New York Avenue, N.W.  
Suite 600  
Washington, D.C. 20005-3934  
(202) 371-2600

**Version with markings to show changes made**

***In the Claims:***

Please amend the following claims:

1. (Twice Amended) An integrated circuit inductor comprising:

a substrate;

a spiral inductor metalization pattern disposed on the substrate including a plurality of parallel tracks in a spiral pattern each track having a first end and a second end and having the first ends coupled together and the second ends coupled together; and

a n<sup>+</sup> diffusion layer disposed in the substrate directly underneath [beneath] the spiral inductor metalization pattern.

10. (Twice Amended) The integrated circuit inductor of claim 1, in which the n<sup>+</sup> diffusion layer [is formed in] has a fingered pattern shape [from n<sup>+</sup> material having] with n<sup>+</sup> fingers electrically isolated by regions of polysilicon [to produce the fingered pattern].

14. (Twice Amended) An integrated circuit inductor comprising:

a substrate having a first layer and a second layer;

a first track disposed on the first layer in a first spiral pattern and having a first input and a first output;

a second track disposed on the second layer in a second spiral pattern and having a second input and a second output, the second spiral pattern oriented parallel to the first spiral pattern; and

a pattern of via holes sufficient to couple a varying voltage present along the length of the first track on to the second track[.];

the first and second inputs connected together by a first via hole of the pattern of via holes, and the first and second outputs connected together by a second via hole of the pattern of via holes.